Docket No. 200309963-1

Remarks

This Amendment is responsive to the **March 13, 2006** Office Action. Reexamination and reconsideration of **claims 1-28** is respectfully requested.

Summary of The Office Action

Claims 1, 3-4, 7, 11, 17, 24-25, and 27 were rejected under 35 U.S.C. §102(e) as being anticipated by Figure 1 of the present specification.

Claims 5, 6, 12-15, 20-23, 26, and 28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Figure 1 of the present specification.

Claims 2 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Figure 1 of the present specification as applied to claims 1, 11, and 13 above, and further in view of De Rooij et al. (2004/0125618).

Claims 8-10, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 1 of the present specification as applied to claims 1 and 17 above, and further in view of Barnsdale, Jr. et al. (4,685,056).

The Present Amendment

Claim 11 has been amended to more particularly claim an output voltage from isolated converter(s) as an input to one non-isolated converter within a first group of non-isolated converters and as an input to one non-isolated converter within a second group of non-isolated converters. No new matter has been added by this amendment. Support for the amendment can be found, for example, at Figure 3 and paragraphs 27-30.

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The Claims Patentably Distinguish Over the References of Record

Independent Claim 1

Claim 1 recites an interleaved intermediate bus configured to supply independent and redundant input to a second set of power converters from one or more power levels of a first set of power converters. The prior art (Fig. 1) fails to teach or suggest these features and thus the section 102 rejection is not supported by Figure 1 since each and every feature of claim 1 is not taught.

Figure 1 of the subject application illustrates a prior art example of power system design and an intermediate bus architecture. (see Specification, Paragraph 5). The design uses an intermediate bus power architecture configured with a common intermediate bus **100** that supplies power from a first set of power converters (e.g., isolated converters **105**) to a second set of power converters (e.g., non-isolated converters **110**). (Paragraph 1). Non-isolated converters **110** operate from the common voltage on the intermediate bus **100**. (Paragraph 1). However, extending this architecture to an N+1 application required additional components to isolate the non-isolated converters **110** from power component failures that can disturb the common intermediate bus voltage period. (Paragraph 1). Thus, the prior art of Figure 1 teaches a common intermediate bus **100**. The outputs of isolated intermediate bus converters **105**, after isolation with isolation diodes **130**, supply power to the common intermediate bus **100** which then supplies the non-isolated converters **110**.

The Office Action states that the prior art (Fig. 1) teaches: "an interleaved intermediate bus (**130**) to supply independent and redundant input to the second set of converters from the first set of converters". (Office Action, page 2, paragraph 2). As discussed above, the intermediate bus **100** of Fig. 1 is a common intermediate bus and not an interleaved bus. Further, reference number **130** refers to an isolation diode **130**, which isolates the isolated intermediate bus converter **105** from the common intermediate bus **100**. Therefore, diode **130** is not even a bus and thus cannot support the present rejection that is

based on an interpretation that diode **130** teaches an interleaved intermediate bus (see Office Action, page 3, line 1). One of ordinary skill in the art clearly understands that a diode is not a bus.

Applicants' representative has reviewed the referenced sections and respectfully submits that the prior art (Fig. 1) does not teach an interleaved intermediate bus configured to supply independent and redundant input to a second set of power converters from one or more output power levels of a first set of power converters. Instead, the outputs of the first set of power converters (isolated intermediate bus converter **105**) are joined (after isolation with isolation diodes **130**) to form a common intermediate bus **100** with the second set of power converters (non-isolated converters **110**) operating from the common voltage on the intermediate bus **100**. (Paragraph 1). The common intermediate bus is not interleaved and is not configured to supply independent and redundant input. This is a different type of bus architecture. In fact, with the common intermediate bus **100**, each of the non-isolated converters **110** is at least partially reliant on the output of each of the isolated intermediate bus converters **105**. Therefore, Figure 1 of the present application fails to teach or suggest the elements of claim 1.

Since Claim 1 recites features not disclosed or suggested by the references, Claim 1 patentably distinguishes over the references of record and is now in condition for allowance. Accordingly, dependent Claims 2-10 also patentably distinguish over the reference and are in condition for allowance.

Dependent Claim 5

Dependent Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art (Fig. 1). Claim 5 recites the interleaved intermediate bus includes outputs from the first set of power converters being operably connected to inputs of the second set of power converters forming multiple independent buses. The Office Action states that this limitation is not taught by the prior art but "it would have been obvious to one of ordinary skill in the art at the time of the invention to form the intermediate bus into multiple

independent buses...since it has been held that rearranging parts in an invention involves only routine skill in the art."

Applicant respectfully submits that the claimed interleaved intermediate bus forming multiple independent buses is a different type of bus architecture, includes different connections to different selected components, and provides different functionality over the prior art. Therefore, this is not simply "rearranging of parts" because different parts and different functions are present. Thus, this rationale for the rejection does not apply to the present claims. If this rationale were applied to inventions that create a new circuit, then all new circuits would be simply a rearranging of parts and no patents would be issued for new circuitry. This, of course, is not the case and the rejection should be withdrawn.

Furthermore, MPEP section 2144.04(VI)(C) provides:

> However "the mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claim on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of applicant specification, to make the necessary changes in the reference." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351,353 (Bd.Pat.App. & Inter. 1984). (Emphasis added).

Prior art Figure 1 is directed to a common intermediate bus **100** and provides no motivation or reason to make the changes proposed by the Office Action. The only motivation comes from the present specification. Therefore, there is no motivation to rearrange outputs of the isolated intermediate bus converter **105** to form multiple independent buses. Absent such motivation, a proper obviousness rejection has not been established. The rejection, thus, is not supported by the reference and should be withdrawn. Dependent claim 5 patentably distinguishes over the references of record for this additional reason.

Independent Claim 11

Claim 11 recites an intermediate power bus architecture configured to provide an output voltage from one or more isolated converters from a set of isolated converters as an independent input voltage to one non-isolated converter within a first group of non-isolated converters and independent input voltage to one non-isolated converter within the second group of non-isolated converters. The prior art (Fig. 1) fails to teach or suggest these features and thus the section 102 rejection is not supported by the prior art since each and every feature of claim 11 is not taught.

The prior art (Fig. 1) discloses a common intermediate bus **100** that supplies power from a first set of power converters (e.g., isolated converters **105**) to a second set of power converters (e.g., non-isolated converters **110**). (Paragraph 1). The non-isolated converters **110** operate from the common voltage on the intermediate bus **100**. (Paragraph 1). Thus the prior art operates with a common intermediate bus configuration and does not disclose an interleaving in which an output of an isolated converter is input to one non-isolated converter within a first group and one non-isolated converter within a second group of non-isolated converters. The common intermediate bus is a different type of bus architecture that fails to teach or suggest the claimed architecture and thus fails to support the rejection.

Dependent Claim 12 recites the intermediate power bus architecture includes multiple independent buses configured to provide the output voltage from the set of isolated converters. As noted above, the prior art (Fig. 1) discloses a common intermediate bus 100. The Office Action in fact states that Fig. 1 fails to teach the intermediate bus forming multiple independent buses. (Office Action at page 3). As discussed above, the "rearranging of parts" rationale does not apply to creating a different bus architecture as claimed. Furthermore, the prior art must provide a motivation or reason for a worker in the art, without benefit of the present specification, to make necessary changes in the reference device. *See, Ex parte Chicago Rawhide Mfg. Co.* The prior art (Fig. 1) teaches a common intermediate bus configuration and does not provide the motivation to form multiple independent buses. Absent such motivation, the obviousness rejection is not supported by the reference.

Since Claim 11 recites features not disclosed or suggested by the reference, Claim 11 patentably distinguishes over the reference of record and is now in condition for allowance. Accordingly, dependent Claims 12-16 also patentably distinguish over the reference and are in condition for allowance.

Independent Claim 17

Claim 17 recites inputting multiple intermediate power levels as independent input signals to a first set of power converters including a redundant input signal and interleaving the multiple independent power levels to provide independent input signals to a second set of power converters including a redundant input signal. The prior art (Fig. 1) fails to teach or suggest these features and thus the section 102 rejection is not supported by the prior art since each and every feature of claim 17 is not taught.

The Office Action states that Fig. 1 of the present specification teaches these features. Applicants' representative has reviewed Fig. 1 and respectfully submits that the prior art (Fig. 1) does not teach inputting multiple power levels as independent input signals to a first set of power converters including a redundant input signal. The prior art (Fig. 1) further does not teach interleaving the multiple intermediate power levels to provide independent input signals to a second set of power converters including a redundant input signal.

Instead, as discussed above, the prior art (Fig. 1) teaches a common intermediate bus **100** that supplies power from a first set of power converters (e.g., isolated converters **105**) to a second set of power converters (e.g., non-isolated converters **110**). (Paragraph 1). The non-isolated converters **110** operate from the common voltage on the intermediate bus 100. (Paragraph 1). Furthermore element **130**, which the rejection uses as teaching the interleaved intermediate bus, is actually a diode and thus cannot teach or suggest any type of bus or any method of interleaving.

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Thus, the prior art (Fig. 1) fails to teach or suggest the claimed method of converting power by inputting multiple intermediate power levels as independent input signals to a first set of power converters including a redundant input signal and interleaving the multiple intermediate power levels to provide independent input signals to a second set of power converters including a redundant input signal.

Since Claim 17 recites features not disclosed or suggested by the reference, Claim 17 patentably distinguishes over the reference of record and is now in condition for allowance. Accordingly, dependent Claims 18-20 also patentably distinguish over the reference and are in condition for allowance.

Independent Claim 21

Claim 21 recites operably connecting outputs of a plurality of power converters to inputs of a first group of power converters as independent intermediate buses without including fault protection components and operably connecting selected buses of the independent intermediate buses to separate inputs of the second group of power converters without including fault protection components. The prior art (Fig. 1) fails to teach, suggest or make obvious these features and thus the section 103 rejection is not supported by the prior art since each and every feature of claim 21 is not taught, suggested or made obvious.

Furthermore element **130** shown in figure 1, which the rejection uses as teaching the interleaved intermediate bus, is actually a diode and thus does not and cannot teach or suggest any type of bus or methods of manufacturing any type of bus.

The Office Action states that an intermediate bus forming multiple independent buses would have been obvious in view of the prior art (Fig. 1). As noted previously, with regard to rearrangement of parts, this rationale does not apply and further, the prior art must provide a motivation or reason for the worker in the art to make the necessary changes in the reference device. (*See, Ex parte Chicago Rawhide Mfg. Co.).* The prior art (Fig. 1) teaches a

common intermediate bus **100** and does not provide the motivation to form independent intermediate buses. Absent such motivation, the obviousness rejection is not supported by the reference.

Dependent Claim 22 further recites connecting each of the independent intermediate buses as a one-to-one relationship with each power converter in the first group of power converters, and as a one-to-one relationship with each power converter in the second group of power converters. This feature is neither taught, suggested, or made obvious by the reference since a common bus fails to teach or suggest any type of one-to-one relationship.

Similarly, dependant Claim 23 recites where the operably connecting forms an interleaved power bus including the independent intermediate buses. This feature is neither taught, suggested, or made obvious by the reference in view of the previous explanations of figure 1.

Since Claim 21 recites features not disclosed, suggested, or made obvious by the reference, Claim 21 patentably distinguishes over the reference of record and is now in condition for allowance. Accordingly, dependent Claims 22 and 23 also patentably distinguish over the reference and are in condition for allowance.

Independent Claim 24

Claim 24 recites a bus means for redundantly connecting a first power converter means to a second power converter means and to supply the intermediate power level as interleaved independent input signals to the second power converter means. The prior art (Fig. 1) fails to teach or suggest this feature and thus the Section 102 rejection is not supported by the prior art reference since each and every feature of Claim 24 is not taught.

As noted above, the prior art reference (Fig. 1) teaches a common intermediate bus **100** that supplies power from a first set of power converters (e.g., isolated converters **105**) to

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a second set of power converters (e.g., non-isolated converters **110**). (Paragraph 1). The non-isolated converters **110** operate from the common voltage on the intermediate bus **100** (Paragraph 1). The prior art reference (Fig. 1) fails to teach or suggest a bus means for redundantly connecting a first power converter means to a second power converter means and to supply the intermediate power level as interleaved independent input signals to the second power converter means.

As previously stated, element **130** shown in figure 1, which the rejection uses as teaching the interleaved intermediate bus, is actually a diode and thus does not and cannot teach or suggest any type of bus or bus means as claimed.

Since Claim 24 recites features not disclosed or suggested by the reference Claim 24 patentably distinguishes over the reference of record and is now in condition for allowance. Accordingly, dependent Claims 25-28 also patentably distinguish over the references and are in condition for allowance.

Conclusion

For the reasons set forth above, **claims 1-28** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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PETER KRAGULJAC (Reg. No. 38,520)
(216) 348-5843
McDonald Hopkins Co., LPA
600 Superior Avenue, E.
Suite 2100
Cleveland, OH 44114